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REMARKS

Claims 1-15 are pending in the application. Applicants amend the specification and claims 1, 5, and 13-15 for clarification. No new matter has been added.

The Examiner objected to Figs. 7 and 10 for not including the legend "Prior Art" because only that which is old is illustrated. Applicants respectfully submit that these figures illustrate eye patterns that are used to explain the functions of the present invention, and are therefore, not admitted as prior art.

The Examiner also objected to Fig. 11 for not including designations "E," "H," and "L" described on page 18 of the specification. Applicants amend the specification to refer to Fig. 10 for the illustration of eye pattern "E" and to clarify "H" and "L" as "high" and "low" levels, which would be readily apparent to one skilled in the art in viewing Fig. 11.

In view of the above, Applicants respectfully request that the Examiner withdraw the objections to the drawings.

The Examiner objected to the disclosure in the specification for apparent informalities. Applicants amend the paragraphs on page 18, lines 3-8 and page 24, lines 3-10 of the specification to correct the noted informalities and to clarify the disclosure. Accordingly, Applicants respectfully request that the Examiner withdraw the objection to the disclosure in the specification.

Claims 13 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,040,738 to Uchida; claim 13 also stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,728,526 to Yamada. Applicants respectfully traverse the rejections.

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The Examiner applied the description of phase-locked loop ("PLL") circuits—element 5 in Fig. 4 of Uchida and element 9 in Fig. 1 of Yamada—in the cited references as alleged disclosure of the claimed invention. Applicants respectfully submit that the division ratios of the respective PLL's in the cited references is given by a circuit external to the PLL—i.e., control section 11 of Uchida and control circuit 5 of Yamada. As such, these external circuits specifying the division ratios do not relate to the VCO control voltages of the respective PLL's. And therefore, Uchida and Yamada, as cited and relied upon by the Examiner, fail to disclose,

“[a] clock timing extraction circuit extracting a clock timing from an input signal, comprising:
phase comparing means for comparing a phase of the input signal and that of a frequency-divided clock to thereby detect a phase difference;
averaging means for averaging the phase difference to thereby generate a control voltage;
voltage-controlled oscillation means for oscillating a synchronizing clock based on the control voltage;
frequency-dividing means for dividing the frequency of the synchronizing clock to generate the frequency-divided clock; and
phase-locked loop control means for determining whether the control voltage falls within a set range to determine whether a phase-locked loop is in a locked state and dynamically setting the frequency-dividing ratio based on said determination,” as recited in claim 13. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 13 is patentable over Uchida and Yamada for at least the above-stated reasons.

Claim 14 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,896,391 to Solheim et al.; claims 1, 2, and 5-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Solheim et al. in view of Uchida; claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Solheim et al. in view of Uchida, and further in view of U.S. Patent 6,741,668 to Nakamura et al.; claim 4 stands rejected under 35 U.S.C. § 103(a) as

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being unpatentable over Solheim et al. in view of Uchida, and further in view of U.S. Patent No.

4,625,180 to Itaya et al.; and claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,538,786 to Naito in view of Solheim et al. and Uchida. Applicants amend claims 1, 5, and 14-15 in a good faith effort to clarify the invention as distinguished from the cited references. Applicants respectfully traverse the rejections.

The Examiner relied upon the description of a data regenerator 50 in Solheim et al. as alleged disclosure of the claimed regeneration control. Solheim et al. describe a technique to find an optimal operation point from a map representing bit error ratios ("BER") at various points of signal voltage and phase. The system described in Solheim et al. relies upon the distribution of BER on the map to identify an optimal operation point. In contrast, the claimed invention provides for a technique that does not use BER or the like to find an optimal point, but relies upon whether signal logic levels measured at adjacent points on a voltage-phase plane match with each other. Applicants refer to Fig. 11 and the "O" and "X" illustrated therein for an exemplary embodiment of this claimed feature.

Therefore, Solheim et al., as cited and relied upon by the Examiner, fail to disclose,

"[a] regeneration control circuit performing a regeneration control of an input signal, comprising:
voltage threshold level setting means for making a decision on the input signal by using a voltage threshold level and generating measured data from the input signal;
clock phase setting means for setting a phase of a clock for decision making;
level decision control means for determining whether signal logic levels of the measured data at adjacent monitor points match with each other, and providing the result of said determination as decision information;
decision information hold means for holding the decision information; and
optimal point setting means for identifying a decision point within a valid zone of an eye pattern at which there is the least

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possibility that error occurs from the decision information obtained by sequentially sweeping the voltage threshold level and the phase of the clock with respect to the input signal and performing the regeneration control in which the decision point thus identified is used as an optimal point," as recited in claim 14. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 14 is patentable over Solheim et al. for at least the above-stated reasons.

Claims 1 and 15 incorporate features that correspond to those of claim 14 cited above. The Examiner relied upon additional references to specifically address the additional features recited in these claims. As such, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine the additional references, the combinations would still have failed to cure the above-described deficiencies of Solheim et al. with respect to claim 14. Accordingly, Applicants respectfully submit that claims 1 and 15, together with claims 2-12 dependent from claim 1, are patentable over the cited references for at least the foregoing reasons with respect to claim 14.

The above statements on the disclosures in the cited references represent the present opinions of the undersigned attorney. The Examiner is respectfully requested to specifically indicate those portions of the respective reference that provide the basis for a view contrary to any of the above-stated opinions.

Applicants appreciate the Examiner's implicit finding that the additional references made of record, but not applied, do not render the claims of the present application unpatentable, whether these references are considered alone or in combination with others.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider

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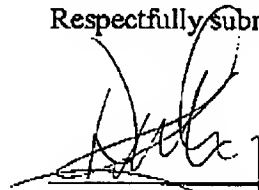
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this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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